14th IEEE International Multitopic Conference (INMIC2011)
December 22 - 24, 2011

# Design of a 19-22GHz Wideband LNA in 0.13µm CMOS Technology using Transmission Lines

Faiza Zafar[1,*], Sana Arshad[1] and Qamar-ul Wahab[1, 2]

[1]Department of Electronic Engineering, NED University of Engineering and Technology, Karachi-75270, Pakistan

[2]Departments of Physics, Chemistry and Biology, Linköping University, SE-581 83, Linköping, Sweden



*faizazafar@ieee.org

# OUTLINE

- Motivation & Objectives
- Introduction & Applications of LNA
- Low Noise Amplifier (LNA) Specifications
- Common Wideband LNA Topologies
- Resistive Feedback Topology
- Design Methodology
- Schematic Design
- Layout Design & Post-Layout Simulation Results
- Comparison with State-of-the-art +15GHz LNAs
- Conclusion & Future Prospects

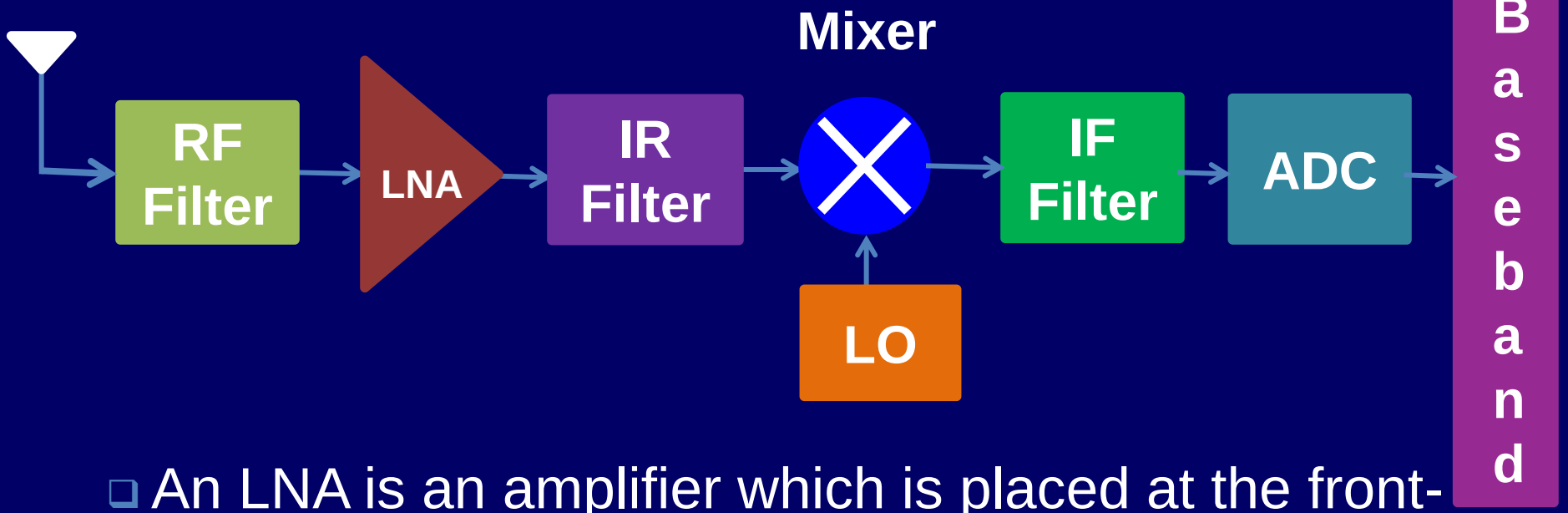
# MOTIVATION

- Obtain performance comparisons among various wideband topologies
- Learn new approaches to the challenges of small-area fully integrated design
- Understand the design considerations of RF front-ends, particularly RF receivers & LNAs
- Learn the optimization & implementation techniques for wideband LNA design in the domain of microwave frequencies

# OBJECTIVES

- To develop a wideband LNA in IBM 0.13µm CMOS technology using Cadence software
- To have a fully integrated transmission line based design in small area
- To obtain LNA specifications better than or at least comparable to state-of-the-art LNA designs

# INTRODUCTION




- An LNA is an amplifier which is placed at the front-end of an RF receiver
- Its main task is to lower the NF of the receiver. Per Friis' formula:

$$NF_{total} = NF_{LNA} + \frac{NF_{other} - 1}{G_{LNA}}$$

# APPLICATIONS

- Cellular Communication
- Biomedical Telemetry
- Radio Astronomy
- Military
- Broadcast industry
- Wireless Computer Networking

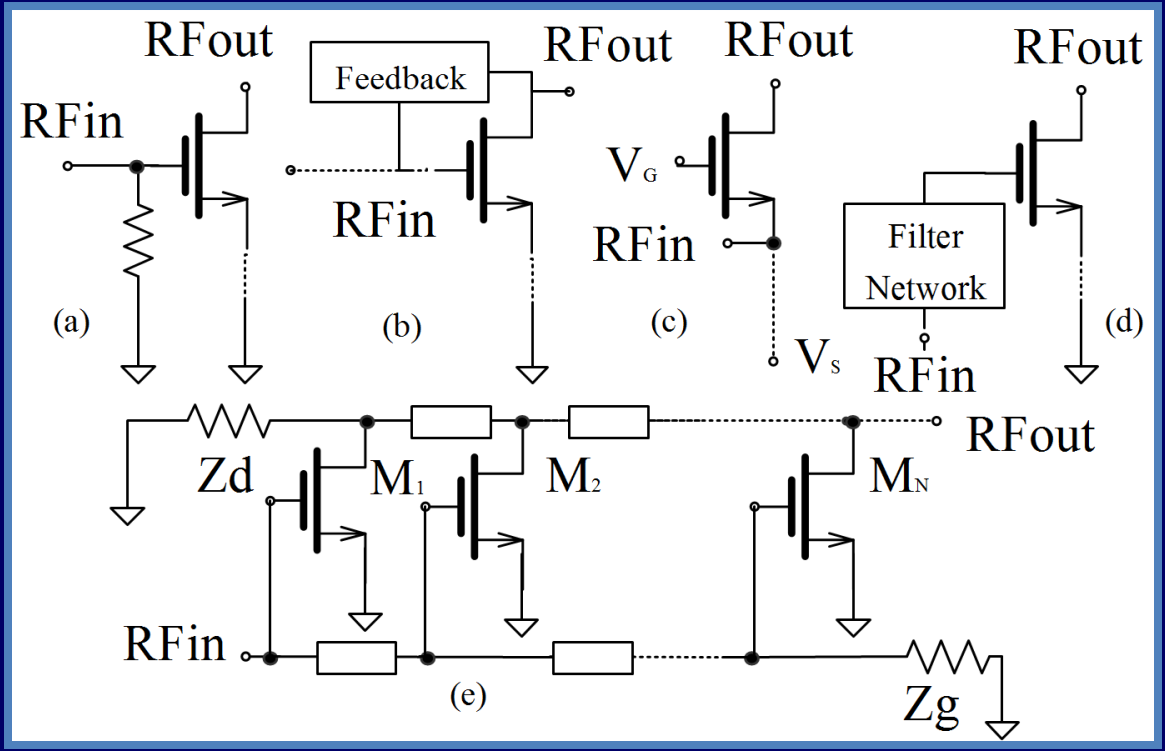


# LNA SPECIFICATIONS

- Gain
- Impedance Matching (Input and Output)
- Noise Figure (NF)
- Unconditional Stability
  - K (Rollet's Stability Factor)
  - $\Delta$ or $B_{1f}$ (Alternate Stability Factor)
- Bandwidth & Centre Frequency
- Linearity
  - Third Order Intercept Point (IP3)
  - 1dB Compression Point ($P_{1dB}$)
- Power Dissipation
- Chip Area Considerations

→ S11
→ S12
→ S21
→ S22

# COMMON WIDEBAND LNA TOPOLOGIES




(a) Common Source with resistive termination (b) Feedback (c) Common Gate (d) Filter LNA (e) Distributed

# RESISTIVE FEEDBACK TOPOLOGY

- Wideband operation because the placement of feedback resistor brings the curve of S11 near the central real axis of Smith chart
- Superior input matching
- Considerably flat gain throughout the bandwidth with smaller degradation of NF
- For low NF, large feedback resistor is required but it places stringent tradeoff between gain and linearity and also hampers flat gain performance

# DESIGN METHODOLOGY

**Step 1**

- Selection of a Transistor
- DC and Transient Analyses

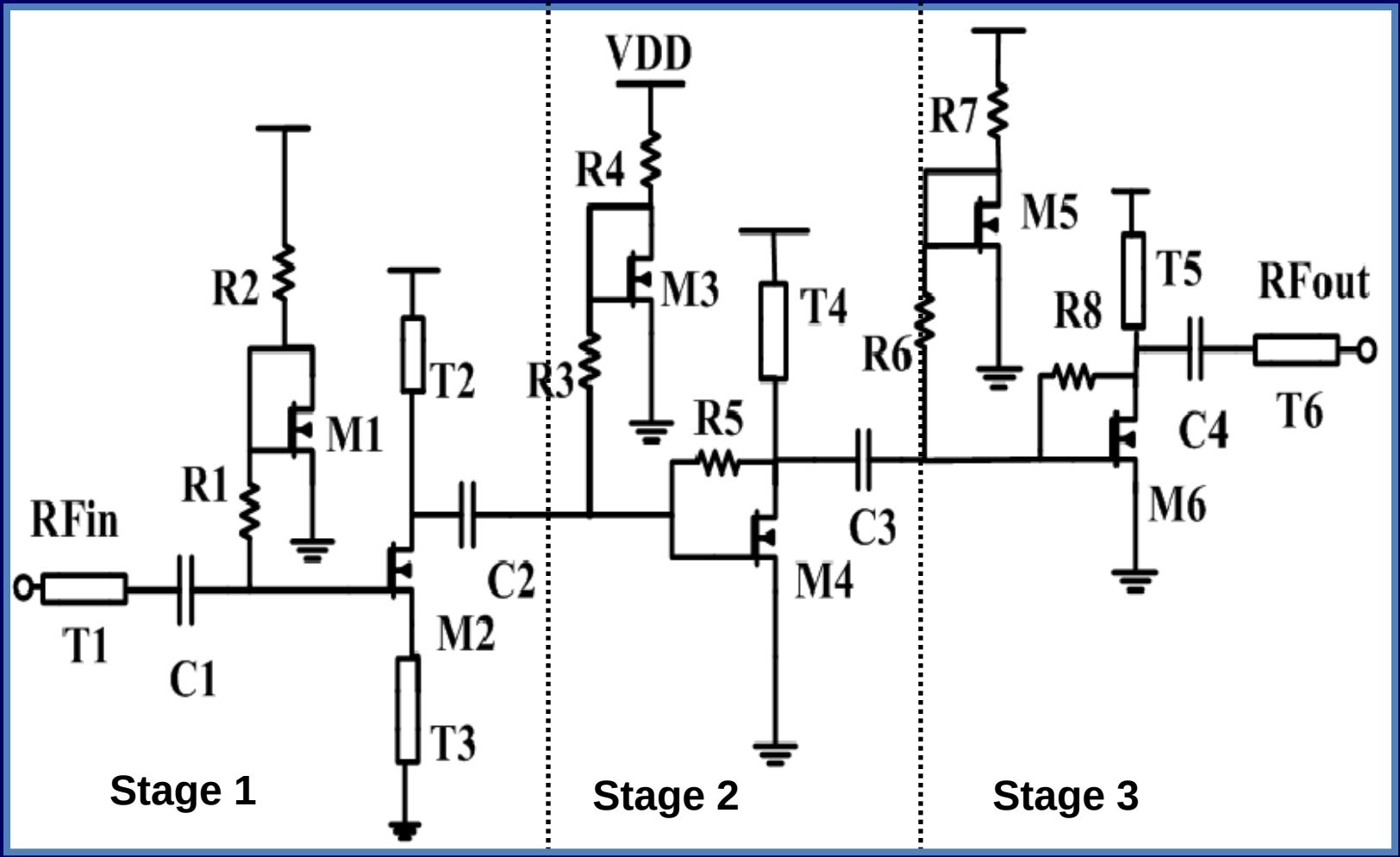
**Step 2**

- Selection of Appropriate Configuration
- S-Parameter Analysis
- Periodic Steady State Analysis
- Optimization of the Configuration

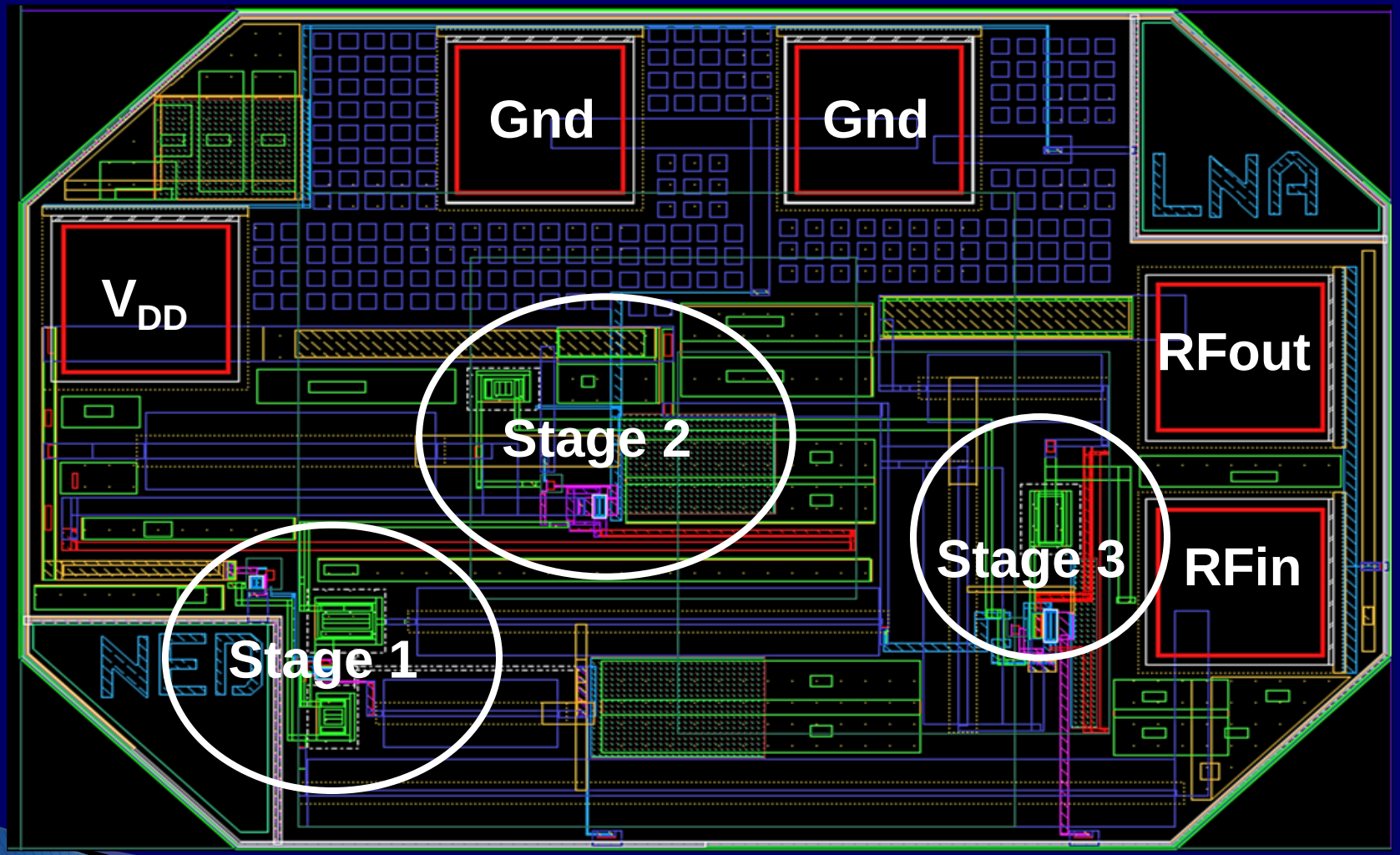
**Step 3**

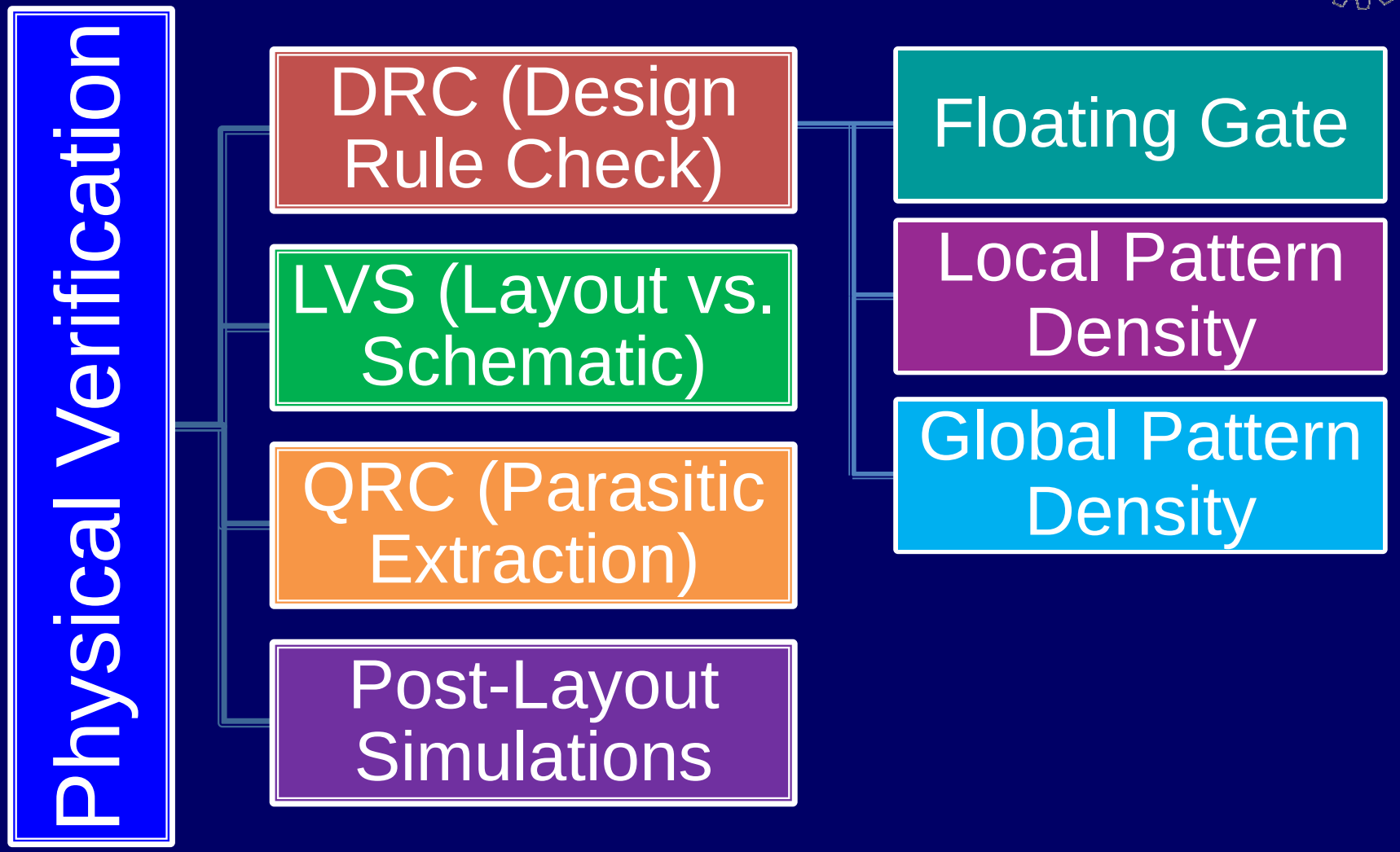
- Layout Design
- Physical Verification

# SCHEMATIC DESIGN

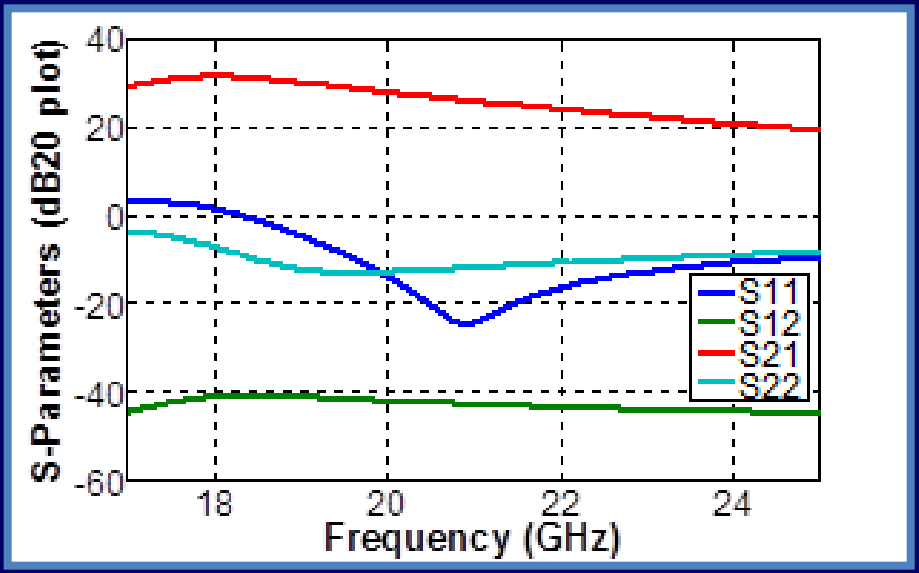


# LAYOUT DESIGN



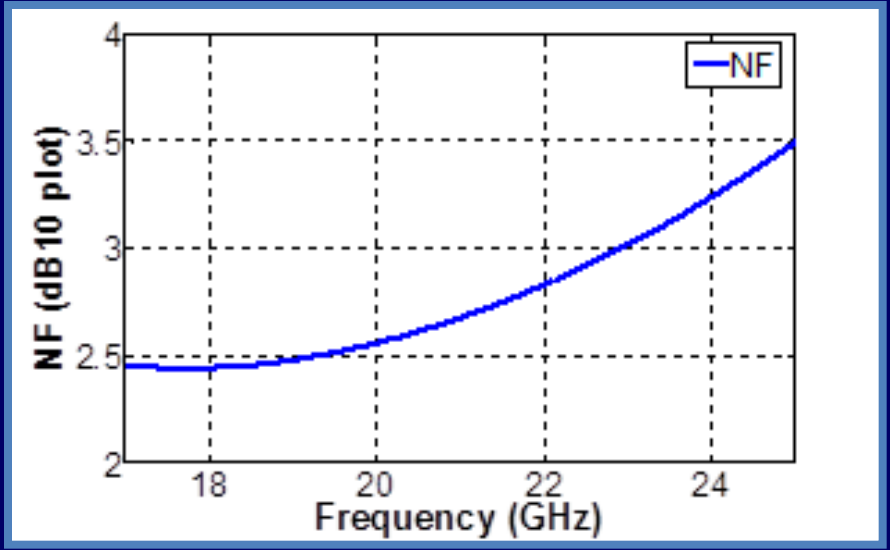

Physical Verification
DRC (Design Rule Check)
LVS (Layout vs. Schematic)
QRC (Parasitic Extraction)
Post-Layout Simulations
Floating Gate
Local Pattern Density
Global Pattern Density

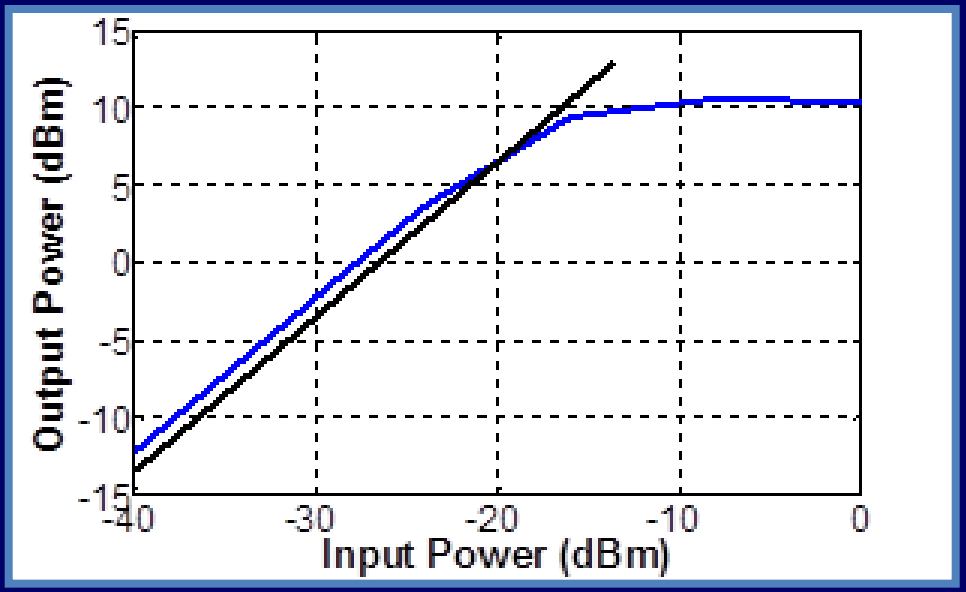
# POST-LAYOUT SIMULATION RESULTS




S-Parameters

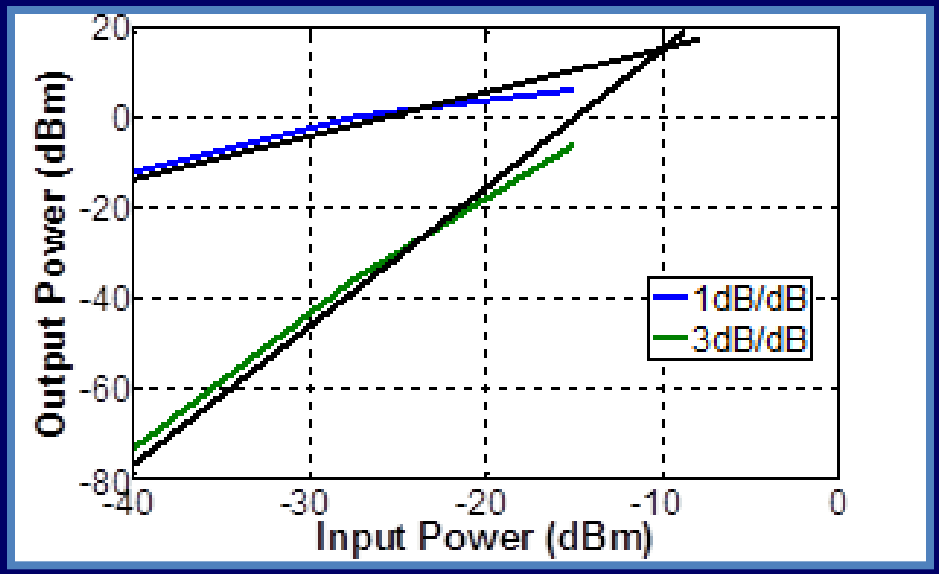
Noise Figure

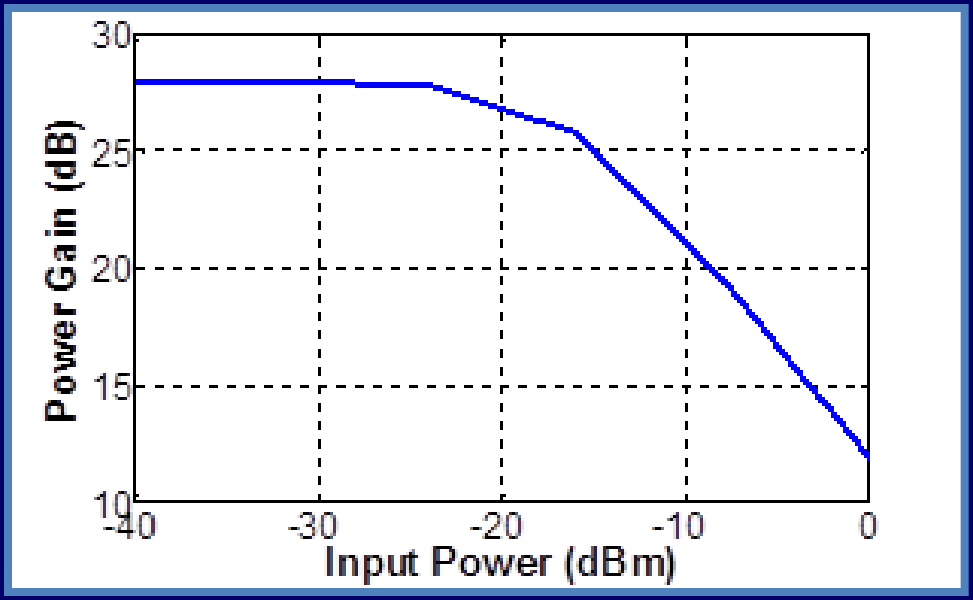





Input Referred $P_{1dB}$ @ 20GHz

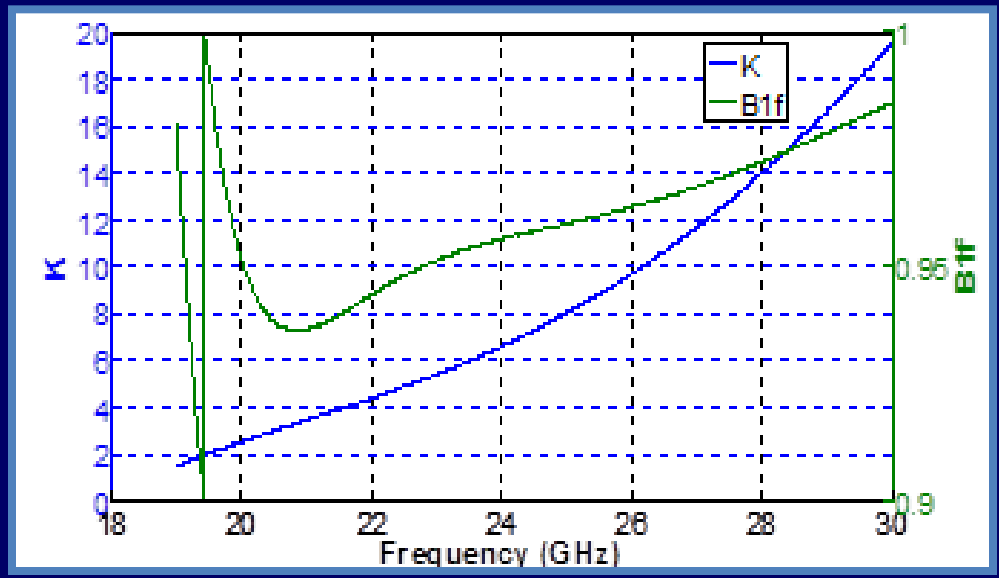
Input Referred IP3 @ 20GHz






Power Gain vs. Input Power

Stability, K > 1 and $B_{1f}$ < 1



# RESULTS

| | |
|---|---|
| S11 | -13dB |
| S12 | -39dB |
| S21 | 27dB |
| S22 | -12dB |
| NF | 2.55dB |
| Input referred P1dB | -21dBm |
| IIP3 | -9.5dBm |
| Power Consumption | 75mW |
| Centre Frequency | 20GHz |
| Bandwidth | 19-22GHz |
| Area* | 0.43mm$^2$ |

*including the chip edge and bond pads

# COMPARISON WITH STATE-OF-THE-ART +15GHz LNAs

| Ref. | Tech µm | $S_{21}$ dB | NF dB | Input P1dB dBm | IIP3 dBm | Power mW | Freq. GHz | Type | FOM |
|---|---|---|---|---|---|---|---|---|---|
| [1] | 0.09 | 8.6 | 3 | - | 5.6 | 19.2 | 20 | Inductor (Lumped) | 10.25 |
| [1] | 0.09 | 12.9 | 2 | - | -2.3 | 19.2 | 15 | Inductor (Lumped) | 3.46 |
| [2] | 0.09 | 5.8 | 6.4 | 1 | 3 | 10 | 20 | TX Lines | 2.31 |
| [2] | 0.09 | 6 | - | -5.75 | - | 19 | 40 | TX Lines | - |
| [3] | 0.09 | 8.8 | 5.2 | - | 7 | 16.8 | 20 | Inductor (Lumped) | 7.11 |
| [4] | 0.18 | 12.9 | 5.6 | -11.1 | 2.04 | 54 | 24 | TX Lines + Inductors | 1.192 |
| [5] | 0.18 | 8.9 | 6.9 | -10.2 | 2.8 | 54 | 26 | TX Lines + Inductors | 0.6555 |
| [5] | 0.18 | 15 | 6 | - | - | 24 | 22 | Inductor (Lumped) | - |
| [6] | 0.18 | 13.1 | 3.9 | -12.2 | 0.54 | 14 | 24 | Inductor (Lumped) | 6.026 |
| [6] | 0.13 | 20 | ~5.5 | -11 | -4 | 24 | 20 | Inductor (Lumped) | 1.301 |
| [7] | 0.18 | 4 | - | - | - | 140 | 39* | Inductor-less (Distributed) | - |
| [8] | 0.18 | 8 | 3.4-5 | - | - | 34 | 0-20 | Distributed (TX Lines + Inductors) | - |
| [9] | 0.18 | 9.3 | 4.4 | -10 | 0.65 | 11.52 | 20 | Inductor (Lumped) | 3.353 |
| **This Work**** | **0.13** | **27** | **2.55** | **-21** | **-9.5** | **75** | **19-22** | **TX Lines** | **0.84** |

FOM=G[abs].IIP3[mW].freq[GHz]/(NF-1)[abs].Pdc[mW]

* Bandwidth

** Simulated Results Only

# CONCLUSION

- A fully integrated LNA for 19-22GHz frequency band is designed in 0.13µm CMOS technology
- It uses cascaded common source amplifiers and resistive feedback technique to obtain wideband operation
- The post-layout simulation results are shown in graphical as well as tabular form and comparison is made with state-of-the-art +15GHz LNAs
- The design is ready for fabrication

# FUTURE PROSPECTS

- The innovation, high speed requirement and compatibility with advanced digital processing systems are the major driving forces of CMOS scaling
- RFIC designers are forced to use the latest technology node for single chip integration and low cost
- Recent technology nodes do not provide precise resistors and thick layer inductors. Therefore, future LNAs must avoid inductors
- Hence, transmission lines can replace inductors to obtain wideband operation without significantly compromising the other LNA specifications such as linearity, gain, noise figure and area

# REFERENCES


[1] L. Aspemyr, H.Jacobsson, M.Bao, H.Sjöland, M. Ferndahl and G. Carchon, “A 15 GHz and a 20 GHz low noise amplifier in 90 nm RF-CMOS”, Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2006.

[2] M. A. Masud, H. Zirath, M. Ferndahl and H.–O. Vickes, “90 nm CMOS MMIC amplifier”, IEEE Radio Frequency Integrated Circuits Symposium, pp. 201-204, 2004.

[3] M. Bao, H. Jacobsson, L. Aspemyr, A. Mercha, and G. Carchon, “A 20GHz sub-1V low noise amplifier and a resistive mixer in 90 nm CMOS technology”, Asia-Pacific Microwave Conference, Vol. 5,China, December 2005.

[4] K.W. Yu and M. F. Chang, ”CMOS K-Band LNAs design counting both interconnect transmission lines and RF pad parasitics”, IEEE Radio Frequency Integrated Circuits Symposium, pp 101-104, 2004.

[5] S.C. Shin et al., “A 24-GHz 3.9-dB NF low-noise amplifier using 0.18μm CMOS technology”, IEEE Microwave and Wireless Components Letter, vol. 15, no. 7, pp. 448-450,July 2005.

[6] G. Xiaoling, and K.O. Kenneth, “A power efficient differential 20-GHz low noise amplifier with 5.3-GHz 3-dB bandwidth”, IEEE Microwave and Wireless Components Letter, vol. 15, no. 9, September 2005.

[7] H. Shigematsu, M. Sato, I. Hirose, F. Brewser and M. Rodwell, “40 Gbps CMOS distributed amplifier for fiber-optic communication systems”, IEEE International Solid-State Circuits Conference, pp. 476–477, 2004.

[8] M.K. Chirala, X. Guan and C. Nguyen, “DC-20 GHz CMOS LNA using novel multilayered transmission lines and inductors”, Electronics Letters, Vol. 42, No. 22, pp. 1273-1275, October 2006.

[9] J.X. Liu, H.C. Kuo, Y.K. Chu, J.F. Yeh, and H.R. Chuang, “A low power 20GHz low noise amplifier fabricated using 0.18μm CMOS technology”, Microwave and Optical Technology Letters, Vol. 51, No. 2, February 2009.

# Thank You

faizazafar@ieee.org

# Q & A